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Docket No. **MSLIN98-002C**

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Sir:

Continuation-In-Part

Transmitted herewith for filing is the Patent Application of:

Inventor: **MOU-SHIUNG LIN**

For: **TOP LAYERS OF METAL FOR HIGH PERFORMANCE IC'S**

02/17/99 jc586 U.S. PTO

jc525 U.S. PTO 09/251183 02/17/99

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[ ] An assignment of the invention to

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Respectfully submitted,

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STATEMENT CLAIMING SMALL ENTITY STATUS (37 CFR 1.9(f) & 1.27(b))--INDEPENDENT INVENTOR

Docket Number (Optional): MSLIN 98-02C

Applicant, Patentee, or Identifier: MOU-SHIUNG LIN

Application or Patent No.: _____

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Title: TOP LAYERS OF METAL FOR HIGH PERFORMANCE IC's

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MOU-SHIUNG LIN		
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January 31, 1999		
Date	Date	Date

MSL98-002C

TOP LAYERS OF METAL FOR HIGH PERFORMANCE IC's

This application is a continuation-in-part application of serial number 09/216,791, filed on December 21, 1998.

BACKGROUND OF THE INVENTION

(1) Field of the invention.

The invention relates to the manufacturing of high performance Integrated Circuit (IC's), and more specifically to methods of achieving high performance of the Integrated Circuits by reducing the parasitic capacitance and resistance of inter-connecting wiring on chip.

(2) Description of the Prior Art.

When the geometric dimensions of the Integrated Circuits are scaled down, the cost per die is decreased while some aspects of performance are improved. The metal connections which connect the Integrated Circuit to other circuit or system components become of relative more importance and have, with the further miniaturization of the IC, an increasingly negative impact on the circuit performance. The parasitic capacitance and resistance of the metal interconnections increase, which

degrades the chip performance significantly. Of most concern in this respect is the voltage drop along the power and ground buses and the RC delay of the critical signal paths. Attempts to reduce the resistance by using wider metal lines result in higher capacitance of these wires.

To solve this problem, the approach has been taken to develop low resistance metal (such as copper) for the wires while low dielectric materials are used in between signal lines.

Increased Input-Output (IO) combined with increased demands for high performance IC's has led to the development of Flip Chip Packages. Flip-chip technology fabricates bumps (typically Pb/Sn solders) on Al pads on chip and interconnect the bumps directly to the package media, which are usually ceramic or plastic based. The flip-chip is bonded face down to the package medium through the shortest path. These technologies can be applied not only to single-chip packaging, but also to higher or integrated levels of packaging in which the packages are larger and to more sophisticated substrates that accommodate several chips to form larger functional units.

The flip-chip technique, using an area array, has the advantage of achieving the highest density of interconnection to

the device and a very low inductance interconnection to the package. However, pre-testability, post-bonding visual inspection, and TCE (Temperature Coefficient of Expansion) matching to avoid solder bump fatigue are still challenges. In mounting several packages together, such as surface mounting a ceramic package to a plastic board, the TCE mismatch can cause a large thermal stress on the solder-lead joints that can lead to joint breakage caused by solder fatigue from temperature cycling operations.

US 5,212,403(Nakanishi) shows a method of forming wiring connections both inside and outside (in a wiring substrate over the chip) for a logic circuit depending on the length of the wire connections.

US 5,501,006(Gehman, Jr. et a].) shows a structure with an insulating layer between the integrated circuit (IC) and the wiring substrate. A distribution lead connects the bonding pads of the IC to the bonding pads of the substrate.

US 5,055,907(Jacobs) discloses an extended integration semiconductor structure that allows manufacturers to integrate circuitry beyond the chip boundaries by forming a thin film

multi-layer wiring decal on the support substrate and over the chip. However, this reference differs from the invention.

US 5,106,461 (Volfson et al.) teaches a multi layer interconnect structure of alternating polyimide (dielectric) and metal layers over an IC in a TAB structure.

US 5,635,767(Wenzel et al.) teaches a method for reducing RC delay by a PBGA that separates multiple metal layers.

US 5,686,764(Fulcher) shows a flip chip substrate that reduces RC delay by separating the power and 1/0 traces.

SUMMARY OF THE INVENTION

It is the primary objective of the present invention is to improve the performance of High Performance Integrated Circuits.

Another objective of the present invention is to reduce resistive voltage drop of the power supply lines that connect the IC to surrounding circuitry or circuit components.

Another objective of the present invention is to reduce the RC delay constant of the signal paths of high performance IC's.

Yet another objective of the present invention is to facilitate the application of IC's of reduced size and increased circuit density.

Yet another objective of the present invention is to further facilitate and enhance the application of low resistor conductor metals.

Yet another objective of the present invention is to allow for increased I/O pin count for the use of high performance IC's.

Yet another objective of the present invention is to simplify chip assembly by reducing the need for re-distribution of I/O chip connections.

Yet another objective of the present invention is to facilitate the connection of high-performance IC's to power buses.

Yet another objective of the present invention is to facilitate the connection of high-performance IC's to clock distribution networks.

Yet another objective of the present invention is to reduce IC manufacturing costs by allowing or facilitating the use of less expensive process equipment and by accommodating less strict application of clean room requirements, this as compared to sub-micron manufacturing requirements.

Yet another objective of the present invention is to be a driving force and stimulus for future system-on-chip designs since the present invention allows ready and cost effective interconnection between functional circuits that are positioned at relatively large distances from each other on the chip.

Yet another objective of the present design is to form the basis for a computer based routing tool that automatically routes interconnections that exceed a pre-determined length in accordance with the type of interconnection that needs to be established.

The present invention adds one or more thick layers of dielectric and one or more layers of wide metal lines on top of

the finished device wafer. The thick layer of dielectric can, for example, be of polyimide or benzocyclobutene (BCB) with a thickness of over, for example, 3 um. The wide metal lines can, for instance, be of aluminum or electroplated copper. These layers of dielectric and metal lines can be used for power buses or power planes, clock distribution networks, critical signal, re-distribution of I/O pads for flip chip applications, and for long signal paths.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 shows a cross section of the interconnection scheme of the present invention.

Fig. 2 shows a cross section of the present invention in a more complex circuit configuration.

Fig. 3a shows the top view of a combination power and X-signal plane using the present invention.

Fig. 3b shows the top view of a combination power and Y-signal plane using the present invention.

Fig. 4 shows the top view of solder bump arrangement using the present invention and is an expanded view of a portion of Fig. 5.

Fig. 5 shows the top view of an example of power/ground pads combined with signal pad using the present invention.

Fig. 6 shows a basic integrated circuit (IC) interconnect scheme of the invention.

Fig. 7 shows an extension of the basic IC interconnect scheme by adding power, ground and signal distribution capabilities.

Fig. 8 shows an approach of how to transition from sub-micron metal to wide metal interconnects.

Fig. 9 shows detail regarding BGA device fan out using the invention.

Fig. 10 shows detail regarding BGA device pad relocation using the invention.

Fig. 11 shows detail regarding the usage of common power, ground and signal pads for BGA devices using the invention.

DETAILED DESCRIPTION OF THE INVENTION

The present invention teaches an Integrated Circuit structure where key re-distribution and interconnection metal layers and dielectric layers are added over a conventional IC. These re-distribution and interconnection layers allow for wider buses and reduce conventional RC delay.

Referring now more specifically to Fig. 1, there is shown a cross section of one implementation of the present invention. A silicon substrate 1 has transistors and other devices, typically formed of poly silicon, covered by a dielectric layer 2 deposited over the devices and the substrate. Layer 3 indicates the totality of metal layers and dielectric layers that are typically created on top of the device layer 2. Points of contact 6, such as bonding pads known in the semiconductor art, are in the top surface of layers 3 and are part of layer 3. These points of contact 6 are points within the IC arrangement that need to be further connected to surrounding circuitry, that is to power lines or to signal lines. A passivation layer 4, formed of for example silicon nitride, is deposited on top of

layer 3, as is known in the art for protecting underlying layers from moisture, contamination, etc.

The key steps of the invention begin with the deposition of a thick layer 5 of polyimide is deposited. A pattern 7 is exposed and etched through the polyimide layer 5 and the passivation layer 4 where the pattern 7 is the same as the pattern of the contact points 6. This opens the contact points 6 up to the surface 8 of the polyimide layer 5.

Electrical contact with the contact points 6 can now be established by filling the openings 7 with a conductor. The tops 9 of this metal conductor can now be used for connection of the IC to its environment, and for further integration into the surrounding electrical circuitry. Pads 10, 11 and 12 are formed on top of the top 9 of the metal conductors 7; these pads can be of any design in width and thickness to accommodate specific circuit design requirements. A larger size pad can, for instance, be used as a flip chip pad. A somewhat smaller in size pad can be used for power distribution or as a ground or signal bus. The following connections can, for instance, be made to the pads shown in Fig. 1: pad 10 can serve as a flip chip pad, pad 11 can serve as a flip chip pad or can be connected to electrical power or to electrical ground or to an electrical

signal bus, pad 12 can also serve as a flip chip pad. There is no connection between the size of the pads shown in Fig. 1 and the suggested possible electrical connections for which this pad can be used. Pad size and the standard rules and restrictions of electrical circuit design determine the electrical connections to which a given pad lends itself.

The following comments relate to the size and the number of the contact points 6, Fig. 1. Because these contact points 6 are located on top of a thin dielectric (layer 3, Fig. 1) the pad size cannot be too large since a large pad size brings with it a large capacitance. In addition, a large pad size will interfere with the routing capability of that layer of metal. It is therefore preferred to keep the size of the pad 6 small. The size of pad 6 is however also directly related with the aspect ratio of via 7. An aspect ratio of about 5 is acceptable for the consideration of via etching and via filling. Based on these considerations, the size of the contact pad 6 can be in the order of 0.5 um. to 3 um. the exact size being dependent on the thickness of layers 4 and 5.

The present invention does not impose a limitation on the number of contact pads that can be included in the design; this

number is dependent on package design requirements. Layer 4 in Fig. 1 can be a typical IC passivation layer.

The most frequently used passivation layer in the present state of the art is plasma enhanced CVD (PECVD) oxide and nitride. In creating layer 4, a layer of approximately 0.2 um. PECVD oxide is deposited first followed by a layer of approximately 0.7 um. nitride. Passivation layer 4 is very important because it protects the device wafer from moisture and foreign ion contamination. The positioning of this layer between the sub-micron process (of the integrated circuit) and the tens-micron process (of the interconnecting metalization structure) is of critical importance since it allows for a cheaper process that possibly has less stringent clean room requirements for the process of creating the interconnecting metalization structure.

Layer 5 is a thick polymer dielectric layer (for example polyimide) that have a thickness in excess of 2 um (after curing). The range of polyimide thickness can vary from 2 um. to 30 um. dependent on electrical design requirements.

For the deposition of layer 5 the Hitachi-Dupont polyimide HD 2732 or 2734 can, for example, be used. The polyimide can be spin-on coated and cured. After spin-on coating, the polyimide

will be cured at 400 degrees C. for 1 hour in a vacuum or nitrogen ambient. For thicker polyimide, the polyimide film can be multiple coated and cured.

Another material that can be used to create layer 5 is the polymer benzocyclobutene (BCB). This polymer is at this time commercially produced by for instance Dow Chemical and has recently gained acceptance to be used instead of typical polyimide application.

The dimensions of opening 7 have previously been discussed. The dimension of the opening together with the dielectric thickness determine the aspect ratio of the opening. The aspect ratio challenges the via etch process and the metal filling capability. This leads to a diameter for opening 7 in the range of approximately 0.5 um. to 3.0 um. while the height for opening 7 can be in the range of approximately 3 um. to 20 um. The aspect ratio of opening 7 is designed such that filling of the via with metal can be accomplished. The via can be filled with CVD metal such as CVD tungsten or CVD copper, with electro-less nickel, with a damascene metal filling process, with electroplating copper, etc.

It must be noted that the use of polyimide films as inter-level dielectrics has been pursued as a technique for providing partial planarization of a dielectric surface. Polyimides offer the following characteristics for such applications:

- they produce surfaces in which the step heights of underlying features are reduced, and step slopes are gentle and smooth.
- they are available to fill small openings without producing the voids that occur when low-temperature CVD oxide films are deposited.
- the cured polyimide films can tolerate temperatures of up to 500 degrees C. without degradation of their dielectric film characteristics.
- polyimide films have dielectric breakdowns, which are only slightly lower than that of SiO_2.
- the dielectric constant of polyimides is smaller than that of silicon nitride and of SiO_2.
- the process used to deposit and pattern polyimide films is relatively simple.

For all of the above characteristics, polyimides are used and recommended within the scope of the present invention.

Fig. 2 shows how the present invention as indicated in

Fig. 1 can be further extended to include multiple layers of polyimide and, in so doing, can be adapted to a larger variety of applications. The lower level build up of this cross section is identical to the build up shown in Fig. 1 with a silicon wafer 1, the poly silicon layer 2, the metal and dielectric combined layer 3, the passivation layer 4, the polyimide layer 5 and the pads 10 deposited on top of layer 5. The function of the structure that has been described in Fig. 1 can be further extended by depositing another layer of polyimide 14 on top of the previously deposited layer 5 and overlaying the pads 10. Selective etching and metal deposition can further create contact points 12. These contact points 12 can be connected with pads 10 as shown by connector 13. Depositing pads 12 on top of layer 14 can thus further extend this process. These pads 12 can be further customized to a particular application, the indicated extension of multiple layers of polyimides greatly enhances the flexibility and usefulness of the present invention. Additional alternating layers of polyimide and metal lines and/or power or ground planes may be added above layers 12 and 16, as needed.

Figs. 3a and 3b show a top view of one possible use of the present invention. Interconnecting a number of pads 32 that have been created as described creates signal lines 30. Additional contact points such as point 34 can allow signal lines to pass

vertically between layers. The various contact points can, for instance, be created within the surface of a power plane or ground plane 36. The layers within the interconnecting metalization structure of the present invention can contain signal interconnections in the X-direction, signal interconnections in the Y-direction, signal interconnections between X and or Y directions, interconnections to and/or within power and/or ground buses. The present invention further teaches the interconnection of signal lines, power and ground buses between the connected IC's and the top of the metalization system of the present invention.

Fig. 3a shows signal lines formed in the X-direction, Fig. 3b shows signal lines formed in the Y-direction.

Fig. 4 presents yet another application of the present invention. Shown in Fig. 4 is an exploded view of a part of Fig. 5 that presents an area array I/O distribution. Fig. 4 shows pads 41 (on which solder bumps can be created) and an example of a layout of the redistribution of the peripheral pads 41'. The exploded view of Fig. 4 is taken along the line 2-2' shown in Fig. 5, the redistribution of the peripheral pads 41' (see Fig. 4) is, for clarity of overview, not shown in Fig. 5. The power or ground connections can be made to any point that is required on

the bottom device. Furthermore, the power and ground planes can be connected to the power and ground planes of the package substrates. Fig. 4 shows an example of how to use the topmost metal layer to redistribute the peripheral pads 41' to become area array pads 41. The solder bumps can then be created on pads 41.

Fig. 5 shows the top surface of a plane that contains a design pattern of a combination of power or ground pads 52 and signal pads 54. Fig. 5 shows the pad openings in the top dielectric layer. It is to be noted that the ground/power pads 52 are heavier and larger in design relative to the signal pads 54. The present invention ideally lends itself to meeting these differences in design, as they are required within the art of chip and high performance circuit design. The number of power or ground pads 52 shown in Fig. 5 can be reduced is there are power and/or ground planes within the chip. From this it is clear that the package number of I/O's can be reduced within the scope of the present invention which leads to a reduction of the package cost by eliminating common signal/power/ground connections within the package. For instance, a 470 I/O count on a BGA chip can, within the scope of the present invention, be reduced

to a 256 I/O count using the present invention. This results in considerable savings for the overall package.

Fig. 6 shows a basic design advantage of the invention. This advantage allows for the sub-micron or fine-lines, that run in the immediate vicinity of the metal layers 3 and the contact points 6, to be extended in an upward direction 20 through metal interconnect 7', this extension continues in the direction 22 in the horizontal plane of the metal interconnect 26 and comes back down in the downward direction 24 through metal interconnect 7". The functions and constructs of the passivation layer 4 and the insulating layer 5 remain as previously highlighted under Fig. 1. This basic design advantage of the invention is to "elevate" or "fan-out" the fine-line interconnects and to remove these interconnects from the micro and sub-micro level to a metal interconnect level that has considerably larger dimensions and is therefore with smaller resistance and capacitance and is easier and more cost effectively to manufacture. This aspect of the invention does not include any aspect of conducting line re-distribution and therefore has an inherent quality of simplicity. It therefore further adds to the importance of the invention in that it makes micro and sub-micro wiring accessible at a wide-metal level. The interconnections 7' and 7" interconnect the fine-level metal by going up through the

passivation and polymer or polyimide dielectric layers, transverses over a distance on the wide-metal level and continues by descending from the wide-metal level back down to the fine-metal level by again transversing down through the passivation and polymer or polyimide dielectric layers. The extensions that are in this manner accomplished need not to be limited to extending fine-metal interconnect points 6 of any particular type, such as signal or power or ground, with wide metal line 26. The laws of physics and electronics will impose limitations, if any, as to what type of interconnect can by established in this manner where limiting factors will be the conventional limiting factors of resistance, propagation delay, RC constants and others. Where the invention is of importance is that the invention provides much broader latitude in being able to apply these laws and, in so doing, provides a considerably extended scope of the application and use of Integrated Circuits and the adaptation of these circuits to a wide-metal environment.

Fig. 7 shows how the basic interconnect aspect of the invention can further be extended to now not only elevate the fine-metal to the plane of the wide-metal but to also add power, ground and signal distribution interconnects of power, ground and signal planes at the wide-metal level. The wide-metal

interconnect 26 of Fig. 6 is now extended to further include an interconnection with the via 21. In typical IC design, some pads may not be positioned in a location from which easy fan-out can be accomplished to a location that is required for the next step of circuit assembly. In those cases, the BGA substrate requires additional layers in the package construction in order to accomplish the required fan-out. The invention teaches an approach that makes additional layers in the assembling of an IC feasible while not unduly increasing the cost of creating such a multi-layer interface. Ball formation 28 on the surface of interconnect 23 indicates how the invention replaces part of the conventional BGA interconnect function, the solder bump provides for flip chip assembly. This interconnect 28 now connects the BGA device with surrounding circuitry at the wide-metal level as opposed to previous interconnects of the BGA device at the fine-metal level. The wide-metal interconnect of the BGA has obvious advantages of cost of manufacturing and improved BGA device performance. By being able to readily extend the wide-metal dimensions it also becomes possible to interconnect power, ground and signal lines at a wide-metal level thereby reducing the cost and complexity of performing this function at the fine-metal level. The indication of 28 as a ball does not imply that the invention is limited to solder bumps for making

interconnects. The invention is equally applicable to wirebonding for making circuit interconnects.

Fig. 8 further shows a cross section wherein the previous linear construction of the metal interconnection running through the passivation layer and the insulation layer is now conical in form. The sub-micron metal layer 60 is covered with a passivation layer 62, a layer 64 of polyimide or polymer is deposited over the passivation layer 62. The wide metal level 66 is formed on the surface of layer 64. The via 70 is shown as having sloping sides, these sloping sides can be achieved by controlling the photolithography process that is used to created the via 70. The etching of the polyimide or polymer can for instance be done under an angle of about 75 degrees with the following curing being done under an angle of 45 degrees. Also, a photosensitive polyimide or polymer can be used, the cone shape of the via 70 can in that case be achieved by variation of exposure combined with time of exposure combined with angle of exposure. Where non-photosensitive polymer or polyimide is used, a wet etch can be applied that has a gradated faster and longer time etch as the top of the via 70 is being approached. The layer of wide-metal pad 68 is deposited on the surface of the polymer or polyimide layer 64, the wide-metal pad deposition 68

mates with the top surface of the via 70 and is centered on top of this surface.

Figs. 9 through 11 show further detail to demonstrate the concepts of BGA chip ball fan-out, pad relocation and the creation of common ground, power and signal pads.

Fig. 9 shows a cross section 100 of a BGA chip, five balls 101 through 105 are also shown. By using the BGA substrate 106 and the wiring 107 within the substrate 106, it is clear that ball 101 can be repositioned to location 111, ball 102 to location 112, etc. for the remaining solder bumps 103 through 105. It is clear that the separation of contact points 111 through 115 is considerably larger than the separation of the original solder bumps 101 through 105. The BGA substrate 106 is the subject of the invention, this substrate allows for spreading the distance between the contact points or balls of the BGA device to a considerable degree.

Fig. 10 shows the concept of pad relocation. BGA pad 120 can be any of the contact balls 101 through 105. By using the BGA substrate 130 and the wiring 131 that is provided within the substrate, it is clear that the BGA pads can be arranged in a different and arbitrary sequence that is required for further

circuit design or packaging. For instance contact point 101, which is on the far left side of the BGA device 100, is re-routed to location 121 which is on the second far right of the BGA substrate 130. The re-arrangements of the other BGA solder bumps can readily be learned from following the wiring 130 within the substrate 131 and by tracing from solder bump to one of the contact points 122 through 125 of the BGA substrate.

Fig. 11 shows the interconnecting of BGA device solder bumps into common power, ground or signal pads. The BGA chip 100 is again shown with five solder bumps 101 through 105. The BGA substrate 130 contains a wiring scheme that contains in this example three wiring units, one for each for the power, ground and signal bumps of the BGA device. It is clear from Fig. 11 that wire arrangement 132 connects BGA device solder bumps 101, 103 and 105 to interconnect point 138 of the BGA substrate 130. It can further be seen that BGA device solder bump 104 is connected to interconnect point 140 of the BGA substrate by means of the wire arrangement 136, while BGA device solder bump 102 is connected to interconnect point 142 of the BGA substrate by means of the wire arrangement 134. The number of pins required to interconnect the BGA device 100 is in this manner reduced from five to three. It is clear that for more BGA device solder bumps, as is the case for an actual BGA device, the

numeric effect of the indicated wiring arrangement is considerably more beneficial.

Some of the advantages of the present invention are:

1) improved speed of the IC interconnections due to the use of wider metal lines (which results in lower resistance) and thicker dielectrics between the interconnecting lines (which results in lower capacitance and reduced RC delay). The improved speed of the IC interconnections results in improved performance of High Performance IC's.

2) an inexpensive manufacturing process since there is no need for expensive equipment that is typically used in sub-micron IC fabrication; there is also no need for the extreme clean room facilities that are typically required for sub-micron manufacturing.

3) reduced packaging costs due to the elimination of the need for redundant I/O and multiple power and ground connection points that are needed in a typical IC packaging.

4) IC's of reduced size can be packaged and inter-connected with other circuit or system components without limiting the performance of the IC's.

5) since dependence on ultra-fine wiring is reduced, the use of low resistance conductor wires is facilitated.

6) structures containing more complicated IC's can be created because the invention allows for increased I/O pin count.

7) more complicated IC's can be created without the need for a significant increase in re-distribution of package I/O connections.

8) power buses and clock distribution networks are easier to integrate within the design of IC's.

9) future system-on-chip designs will benefit from the present invention since it allows ready and cost effective interconnection between functional circuits that are positioned at relatively large distances from each other on the chip.

10) form the basis for a computer based routing tool that automatically routes interconnections that exceed a pre-determined length in accordance with the type of interconnection that needs to be established.

11) provide a means to standardize BGA packaging.

12) be applicable to both solder bumps and wirebonding for making further circuit interconnects.

13) provide a means for BGA device solder bump fan-out thereby facilitating the packing and design of BGA devices.

14) provide a means for BGA device pad relocation thereby providing increased flexibility for the packing and design of BGA devices.

15) provide a means for common BGA device power, ground and signal lines thereby reducing the number of pins required to interconnect the BGA device with the surrounding circuits.
16) provide a means for more relaxed design rules in designing circuit vias by the application of sloped vias.
17) provide the means for extending a fine-wire interconnect scheme to a wide-wire interconnect scheme without the need to apply a passivation layer over the surface of the fine-wire structure.

Although the preferred embodiment of the present invention has been illustrated, and that form has been described in detail, it will be readily understood by those skilled in the art that various modifications may be made therein without departing from the spirit of the invention or from the scope of the appended claims.

What is claimed is:

1. A method for forming a top metalization system for high performance integrated circuits, comprising:

forming an integrated circuit comprising a plurality of devices formed in and on a semiconductor substrate, with an overlaying interconnecting metalization structure connected to said devices and comprising a plurality of first metal lines in one or more layers;

depositing a passivation layer over said interconnecting metalization structure;

depositing an insulating, separating layer over said passivation layer that is substantially thicker than said passivation layer;

forming openings through said insulating, separating layer and said passivation layer to expose upper metal portions of said overlaying interconnecting metalization structure;

depositing metal contacts in said openings; and

forming said top metalization system connected to said overlaying interconnecting metalization structure, wherein said top metalization system comprises a plurality of top metal lines, in one or more layers, each of said top metal lines having a width substantially greater than said first metal lines.

2. The method of claim 1 wherein the top metalization system connects portions of said interconnecting metalization structure to other portions of said interconnecting metalization structure.

3. The method of claim 1 wherein said top metalization system comprises signal lines that are substantially wider than lines in said interconnecting metalization structure.

4. The method of claim 1 wherein said top metalization system comprises power planes having power buses that are substantially wider than lines in said interconnecting metalization structure.

5. The method of claim 1 wherein said top metalization system comprises ground planes having ground buses that are substantially wider than lines in said interconnecting metalization structure.

6. The method of claim 1 wherein said top metalization system comprises planes that contain both signal lines and power buses that are substantially wider than lines in said interconnecting metalization structure.

7. The method of claim 1 wherein said top metalization system comprises planes that contain both signal lines and ground buses that are substantially wider than lines in said interconnecting metalization structure.

8. The method of claim 1 wherein said top metalization system comprises planes that contain both power buses and ground buses that are substantially wider than lines in said interconnecting metalization structure.

9. The method of claim 1 wherein said overlaying interconnecting metalization structure comprises electrical contact points.

10. The method of claim 9 wherein the size of said contact points is within the range of approximately 0.3 um. to 5.0 um.

11. The method of claim 1 wherein said passivation layer comprises Plasma Enhanced CVD (PECVD) oxide.

12. The method of claim 1 wherein said passivation layer comprises Plasma Enhanced CVD (PECVD) nitride.

13. The method of claim 1 wherein said passivation layer comprises a layer within the range of approximately 0.15 to 2.0

um of Plasma Enhanced CVD (PECVD) oxide over which a layer within the range of approximately 0.5 to 2.0 um PECVD nitride is deposited.

14. The method of claim 1 wherein said insulating, separating layer is a polymer dielectric layer or any other appropriate insulating material.

15. The method of claim 1 wherein said insulating, separating layer comprises polyimide.

16. The method of claim 1 wherein said insulating, separating layer comprises the polymer benzocyclobutene (BCB).

17. The method of claim 1 wherein said insulating, separating layer is of a thickness after curing within the range of approximately 1.0 to 30 um.

18. The method of claim 1 wherein said insulating, separating layer is spin-on coated and cured.

19. The method of claim 1 wherein said insulating, separating layer after said spin-on coating is cured at a temperature within the range of approximately 250 to 450 degrees C. for a time

within the range of approximately 0.5 to 1.5 hours said curing to occur within a vacuum or nitrogen ambient.

20. The method of claim 16 wherein said insulating, separating layer is subjected to multiple processing steps of spin on coating and curing.

21. The method of claim 20 wherein said insulating, separating layer after each process step of said spin on coating is cured at a temperature within the range of approximately 250 to 450 degrees C. for a time within the range of approximately 0.5 to 1.5 hours said curing the occur within a vacuum or nitrogen ambient.

22. The method of claim 1 wherein said openings have an aspect ratio within the range of approximately 1 to 10.

23. The method of claim 1 wherein said metal contacts are selected from a group comprise sputtered aluminum, CVD tungsten, CVD copper, electroplated copper and electroless nickel.

24. The method of claim 1 wherein said metal contacts comprise damascene metal filling.

25. The method of claim 1 wherein said top metalization system comprises contact pads on the top metal layer whereby said contact pad can comprise any appropriate contact material, such as but not limited to tungsten, chromium, copper (electroplated or electroless), aluminum, polysilicon, or the like.

26. The method of claim 1 wherein said top metal layer comprises contact pads, said contact pads comprising signal connection pads whereby said signal connection pads can comprise any appropriate contact material, such as but not limited to tungsten, chromium, copper (electroplated or electroless), aluminum, polysilicon, or the like.

27. The method of claim 1 wherein said top metalization system contains contact pads on the top metal layer, said contact pads containing signal connection pads in addition to power and ground connection pads whereby said signal connection pads can comprise any appropriate contact material, such as but not limited to tungsten, chromium, copper (electroplated or electroless), aluminum, polysilicon, or the like.

28. The method of claim 27 wherein said signal pads are mounted in the periphery of said top metalization system and said power and ground connection pads are mounted within the area enclosed

by said signal pads whereby said power and ground connection pads and said signal pads can comprise any appropriate contact material, such as but not limited to tungsten, chromium, copper (electroplated or electroless), aluminum, polysilicon, or the like.

29. A semiconductor device structure comprising:

a semiconductor substrate comprising semiconductor devices;

an interconnecting metalization structure connected to said devices;

electrical contact points on an upper top surface of said interconnecting metalization structure and connected to said interconnecting metalization structure;

a passivation layer deposited over said interconnecting metalization structure and over said electrical contact points;

an insulating layer deposited over said passivation layer said insulating layer being substantially thicker than said passivation layer;

openings through said insulating layer and through said passivation layer down to the upper surface of said electrical contact points;

metal conductors within said openings; and

an upper metalization structure connected to said metal conductors.

30. The method of claim 29 wherein the upper metalization structure connects portions of said interconnecting metalization structure to other portions of said interconnecting metalization structure.

31. The structure of claim 29 wherein said upper metalization structure further comprises:

a plurality of insulating layers;

a plurality of structures of metal interconnecting lines formed between said insulating layers;

a plurality of contact pads in an upper layer of said metalization structure; and

a plurality of filled openings connecting said contact pads with one or more of said structures of metal interconnecting lines further connecting said contact pads with said electrical contact points.

32. The structure of claim 31 whereby said metal interconnecting lines are signal lines, and are substantially wider than lines in said interconnecting metalization structure.

33. The structure of claim 31 wherein said metal interconnecting lines are power buses, and are substantially wider than lines in said interconnecting metalization structure.

34. The structure of claim 31 wherein said metal interconnecting lines are ground buses, and are substantially wider than lines in said interconnecting metalization structure.

35. The structure of claim 31 wherein said metal interconnecting lines are a combination of signal lines and power buses, and are substantially wider than lines in said interconnecting metalization structure.

36. The structure of claim 31 wherein said metal interconnecting lines are a combination of power and ground buses, and are substantially wider than lines in said interconnecting metalization structure.

37. The structure of claim 31 wherein said metal interconnecting lines are a combination of signal and ground buses, and are substantially wider than lines in said interconnecting metalization structure.

38. The structure of claim 29 wherein the size of said contact points is within the range of approximately 0.3 um. to 5.0 um whereby further whereby said contact points can comprise any appropriate contact material, such as but not limited to

tungsten, copper (electroplated or electroless), aluminum, polysilicon, or the like.

39. The structure of claim 29 wherein said passivation layer comprises a layer within the range of approximately 0.15 to 2.0 um Plasma Enhanced CVD (PECVD) oxide over which a layer within the range of approximately 0.5 to 2.0 um PECVD nitride is deposited.

40. The method of claim 29 wherein said insulating, separating layer is a polymer dielectric layer or any other appropriate insulating material.

41. The method of claim 29 wherein said insulating, separating layer comprises polyimide.

42. The method of claim 29 wherein said insulating, separating layer comprises the polymer benzocyclobutene (BCB).

43. The structure of claim 29 wherein said insulating layer is of a thickness after curing within the range of approximately 1.0 to 30 um.

44. The structure of claim 29 wherein said openings have an aspect ratio within the range of approximately 1 to 10.

45. The method of claim 29 wherein said metal conductors within said openings through said insulating layer and through said passivation layer connecting said electrical contact pads of said top metalization structure with contact points of said interconnecting metalization structure are constructed and routed such that each said electrical contact point of said interconnecting metalization structure is connected directly and sequentially with one electrical contact point of said top metalization structure thereby creating a fan-out effect for said electrical contact point of said interconnecting metalization structure whereby the distance between said electrical contact points of said top metalization structure is larger than the distance between said electrical contact points of said interconnecting metalization structure by a measurable amount.

46. The method of claim 29 wherein said the number of said electrical contact pads of said upper metalization structure can be larger than the number of said contact points of said interconnecting metalization structure by a considerable and measurable amount.

47. The method of claim 29 wherein said metal conductors within said openings through said insulating layer and through said passivation layer connecting said electrical contact points of said top metalization structure with said contact points of said interconnecting metalization structure are constructed and routed such that each said electrical contact point of said interconnecting metalization structure is connected directly but not necessarily sequentially with one electrical contact point of said top metalization structure thereby creating a pad relocation effect for said electrical contact points of said interconnecting metalization structure whereby the distance between said electrical contact points of said top metalization structure is larger than the distance between said electrical contact point of said interconnecting metalization structure by a measurable amount whereby furthermore the sequence or adjacency of said electrical contact points of said interconnecting metalization structure is not necessarily the same as the sequence or adjacency between said electrical contact points of said top metalization structure.

48. The method of claim 29 wherein said metal conductors within said openings through said insulating layer and through said passivation layer connecting said electrical contact points on a top surface of said top metalization structure with contact

points of said interconnecting metalization structure are constructed and routed such that functionally identical electrical contact points of said interconnecting metalization structure are inter-connected and are connected with one electrical contact point or fewer electrical contact points of said top metalization structure thereby creating a reduction effect for said electrical contact points of said interconnecting metalization structure whereby the number of contact points for a particular electrical function within said electrical contact points of said top metalization structure is smaller than the number of said electrical contact points of said interconnecting metalization structure by a measurable amount whereby furthermore the sequence or adjacency of said electrical contact points of said interconnecting metalization structure is not necessarily the same as the sequence or adjacency between said electrical contact points of said top metalization structure.

49. A method for forming a top metalization system for high performance integrated circuits, comprising:
forming an integrated circuit comprising a plurality of devices formed in and on a semiconductor substrate, with an overlaying interconnecting metalization structure connected to said devices and comprising a plurality of first metal lines;

depositing an insulating, separating layer over said semiconductor substrate;

forming openings through said insulating, separating layer to expose upper metal portions of said interconnecting metalization structure;

depositing metal contacts in said openings; and

forming said top metalization system connected to said interconnecting metalization structure, wherein said top metalization system comprises a plurality of top metal lines, in one or more layers, having a width substantially greater than said first metal lines.

50. The method of claim 49 wherein said top metalization system comprises signal lines that are substantially wider than lines in said overlaying interconnecting metalization structure.

51. The method of claim 49 wherein said top metalization system comprises power buses that are substantially wider than lines in said interconnecting metalization structure.

52. The method of claim 49 wherein said top metalization system comprises ground buses that are substantially wider than lines in said interconnecting metalization structure.

53. The method of claim 49 wherein said top metalization system comprises planes that contain both signal lines and power buses that are substantially wider than lines in said interconnecting metalization structure.

54. The method of claim 49 wherein said top metalization system comprises planes that contain both signal lines and ground buses that are substantially wider than lines in said overlaying interconnecting metalization structure.

55. The method of claim 49 wherein said top metalization system comprises planes that contain both power buses and ground buses that are substantially wider than lines in said overlaying interconnecting metalization structure.

56. The method of claim 49 wherein said overlaying interconnecting metalization structure comprises electrical contact points whereby said contact points can comprise any appropriate contact material, such as but not limited to tungsten, copper (electroplated or electroless), aluminum, polysilicon, or the like.

57. The method of claim 56 wherein the size of said contact points is within the range of approximately 0.3 um. to 5.0 um.

58. The method of claim 49 further comprising depositing a passivation layer over said interconnecting metalization structure.

59. The method of claim 58 wherein said passivation layer comprises Plasma Enhanced CVD (PECVD) oxide.

60. The method of claim 58 wherein said passivation layer comprises Plasma Enhanced CVD (PECVD) nitride.

61. The method of claim 49 wherein said insulating, separating layer is a polymer dielectric layer or any other appropriate insulating material.

62. The method of claim 49 wherein said insulating, separating layer is selected from the group comprising polyimide and benzocyclobutene (BCB).

63. A method for forming a top metalization system for high performance integrated circuits, comprising: forming an integrated circuit comprising a plurality of devices formed in and on a semiconductor substrate, with an overlaying interconnecting metalization structure connected to said devices and comprising a plurality of fine-wire metal lines;

depositing a passivation layer over said interconnecting fine-wire metalization structure;

depositing an insulating, separating layer over said passivation layer that is substantially thicker than said passivation layer;

forming openings through said insulating, separating layer to expose upper metal portions of said overlaying interconnecting metalization structure;

depositing metal contacts in said openings thereby raising a plurality of contact points in said overlaying interconnecting metalization structure to the top surface of said insulating, separating layer thereby creating elevated interconnecting metalization contact points;

forming said top metalization system connected to said overlaying interconnecting metalization structure, wherein said top metalization system comprises a plurality of top wide-metal lines, in one or more layers, having a width substantially greater than said fine-wire metal lines, wherein said top metalization system directly interconnects said elevated interconnecting metalization contact points thereby functionally extending or connecting said fine-wire metal interconnects with said wide-wire metal interconnects thereby furthermore establishing electrical interconnects between multiple points within said fine-wire interconnects.

64. The method of claim 63 wherein said top metalization system comprises signal lines that are substantially wider than lines in said interconnecting metalization structure.

65. The method of claim 63 wherein said top metalization system comprises power planes that are substantially wider than lines in said interconnecting metalization structure.

66. The method of claim 63 wherein said top metalization system comprises ground planes that are substantially wider than lines in said interconnecting metalization structure.

67. The method of claim 63 wherein said passivation layer comprises Plasma Enhanced CVD (PECVD) oxide.

68. The method of claim 63 wherein said passivation layer comprises Plasma Enhanced CVD (PECVD) nitride.

69. The method of claim 63 wherein said insulating, separating layer is a polymer dielectric layer or any other appropriate insulating material.

70. The method of claim 63 wherein said insulating, separating layer comprises polyimide.

71. The method of claim 63 wherein said insulating, separating layer comprises the polymer benzocyclobutene (BCB).

72. The method of claim 63 wherein said insulating, separating layer is of a thickness after curing within the range of approximately 1.0 to 30 um.

73. The method of claim 63 wherein said insulating, separating layer is spin-on coated and cured.

74. The method of claim 63 wherein said openings have an aspect ratio within the range of approximately 1 to 10.

75. The method of claim 63 wherein said metal contacts is selected from the group comprising sputtered aluminum, CVD tungsten, CVD copper, electroplated copper, electroless nickel and damascene metal filling.

76. The method of claim 63 wherein said openings through said insulating, separating layer have sloped sides and wherein each of said openings is wider at its top.

77. The method of claim 63 thereby furthermore functionally and physically extending said top metalization system connected to

said overlaying interconnecting metalization structure, wherein said top metalization system comprises a plurality of ground planes, in one or more layers, wherein furthermore said overlaying interconnecting metalization structure directly interconnects a multiplicity of ground wires said ground wires to be connected with fine-wire ground wires thereby functionally extending or connecting said fine-wire ground wire metal interconnects with said wide-wire metal ground wire interconnects contained within said top metalization system thereby extending the fine-wire ground wires as contained within the overlaying interconnecting metalization structure with said top metalization system.

78. The method of claim 63 thereby furthermore functionally and physically extending said top metalization system connected to said overlaying interconnecting metalization structure, wherein said top metalization system comprises a plurality of signal planes, in one or more layers, wherein furthermore said overlaying interconnecting metalization structure directly interconnects a multiplicity of signal wires said signal wires to be connected with fine-wire signal wires thereby functionally extending or connecting said fine-wire signal wire metal interconnects with said wide-wire metal signal wire interconnects contained within said top metalization system thereby extending

the fine-wire signal wires as contained within the overlaying interconnecting metalization structure with said top metalization system.

79. The method of claim 63 thereby furthermore functionally and physically extending said top metalization system connected to said overlaying interconnecting metalization structure, wherein said top metalization system comprises a plurality of power planes, in one or more layers, wherein furthermore said overlaying interconnecting metalization structure directly interconnects a multiplicity of power wires said power wires to be connected with fine-wire power wires thereby functionally extending or connecting said fine-wire power wire metal interconnects with said wide-wire metal power wire interconnects contained within said top metalization system thereby extending the fine-wire power wires as contained within the overlaying interconnecting metalization structure with said top metalization system.

ABSTRACT

A method of closely interconnecting integrated circuits contained within a semiconductor wafer to electrical circuits surrounding the semiconductor wafer. Electrical interconnects are held to a minimum in length by making efficient use of polyimide or polymer as an inter-metal dielectric thus enabling the integration of very small integrated circuits within a larger circuit environment at a minimum cost in electrical circuit performance.

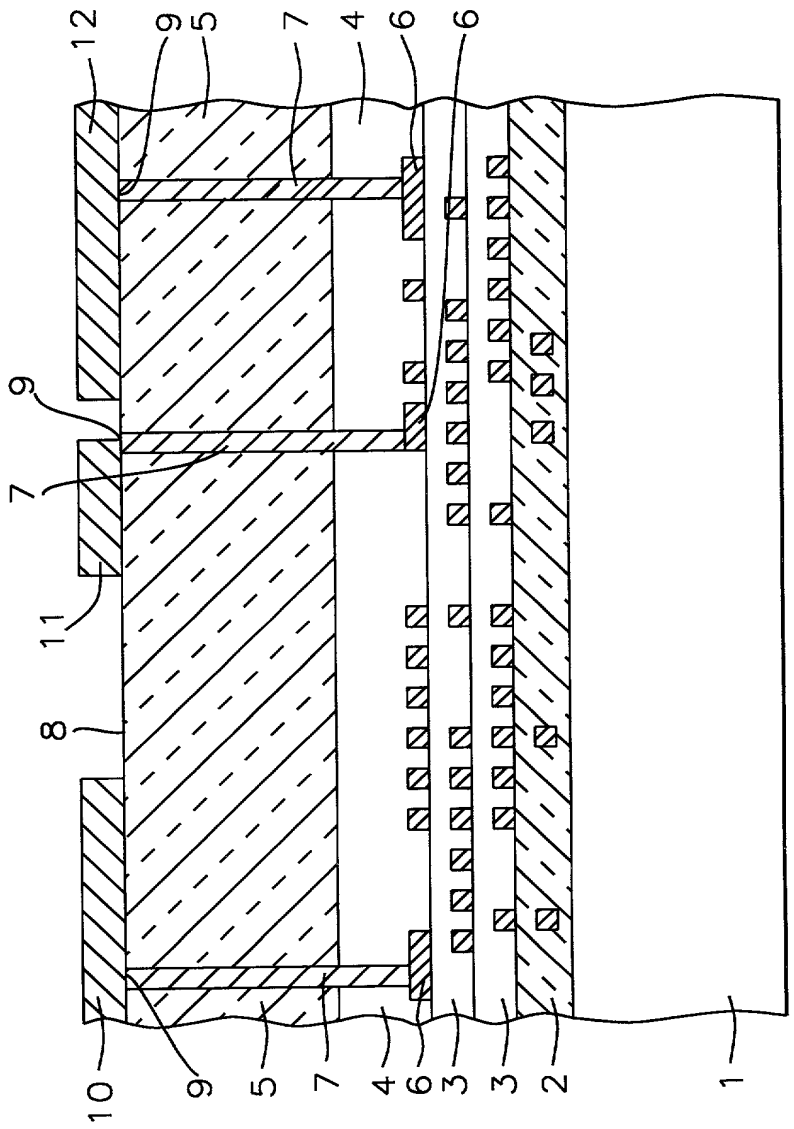

FIG. 1

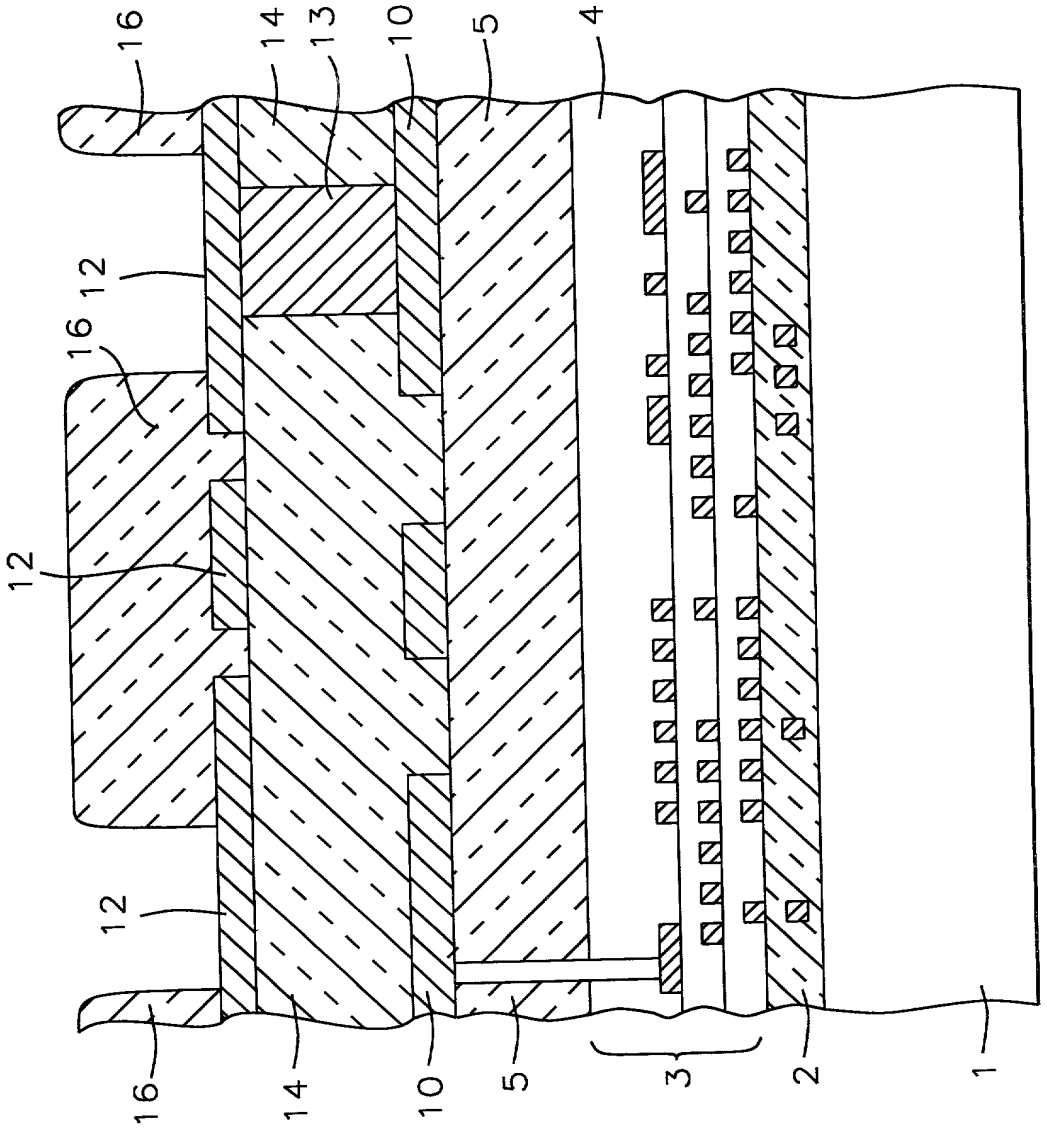

FIG. 2

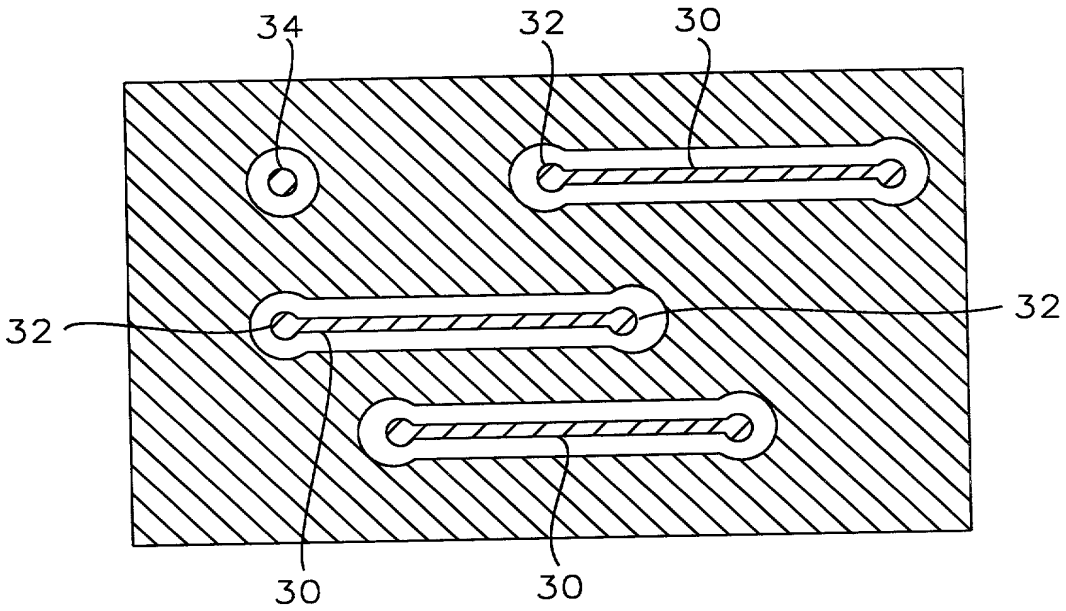

FIG. 3a

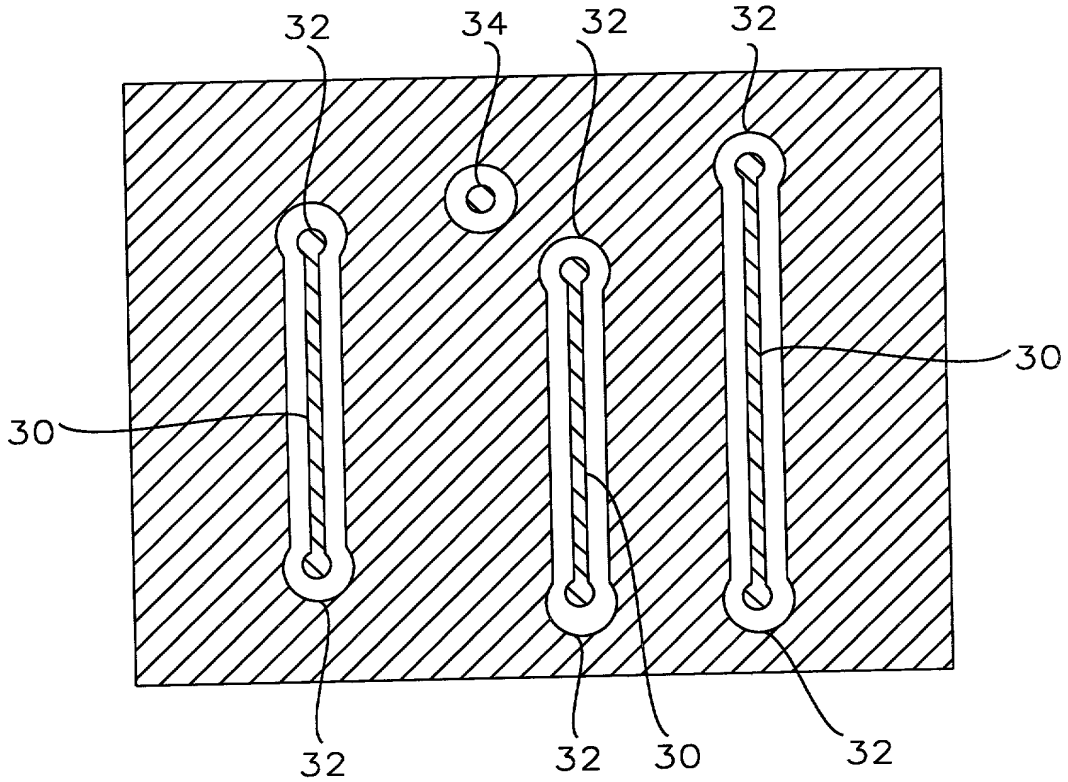

FIG. 3b

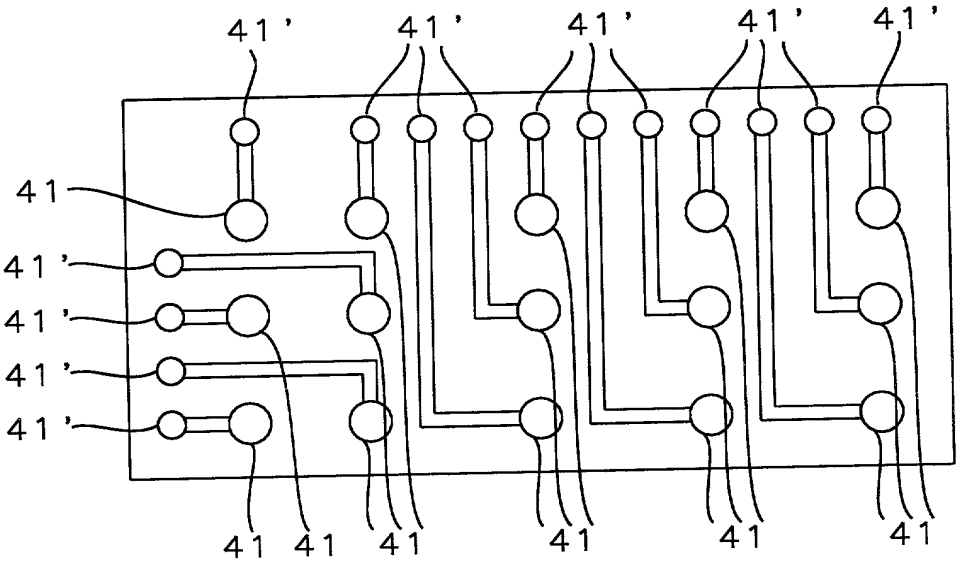

FIG. 4

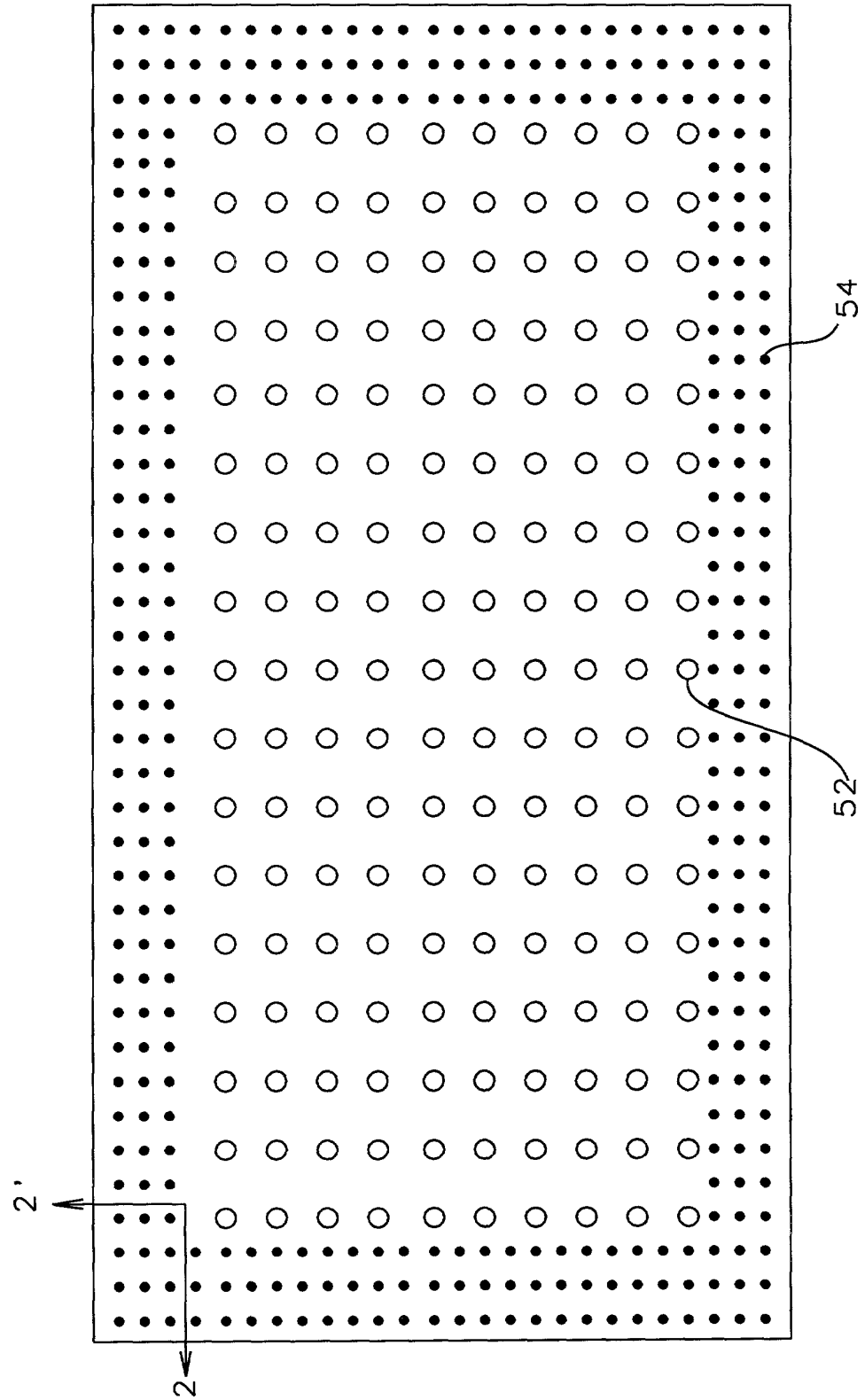

FIG. 5

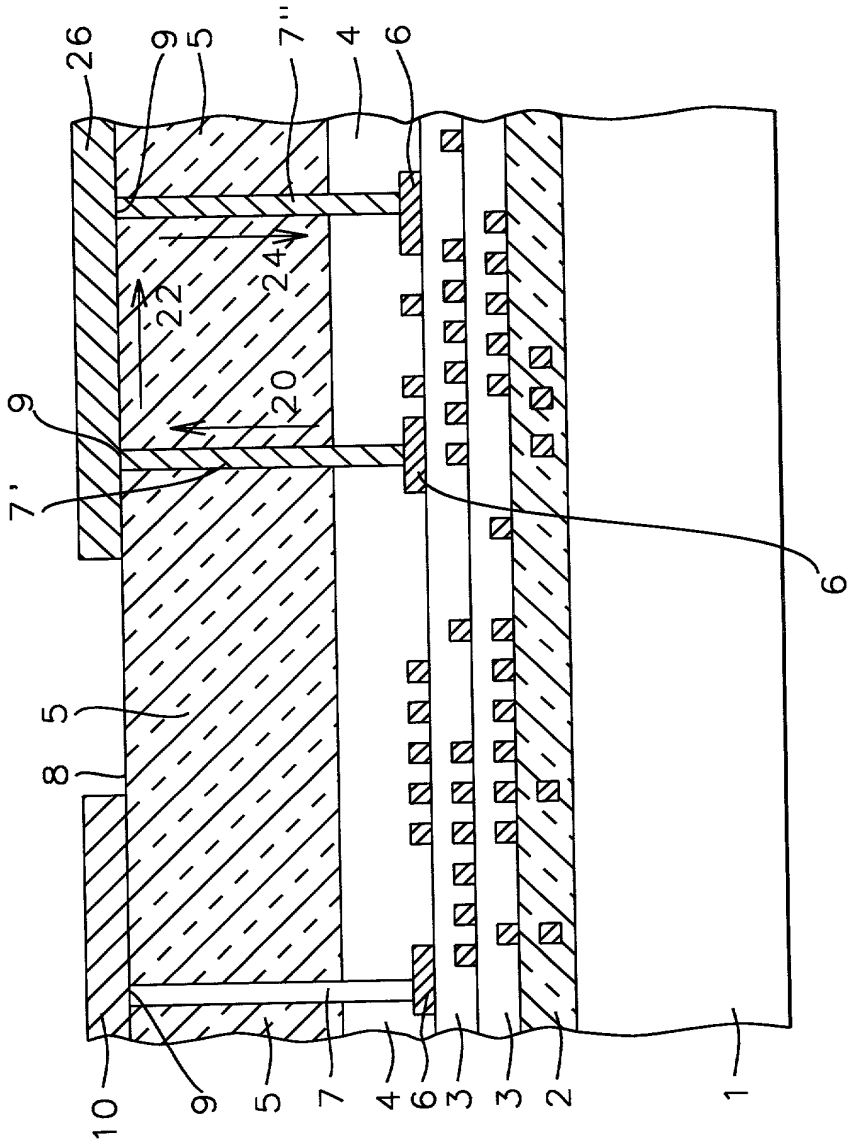

FIG. 6

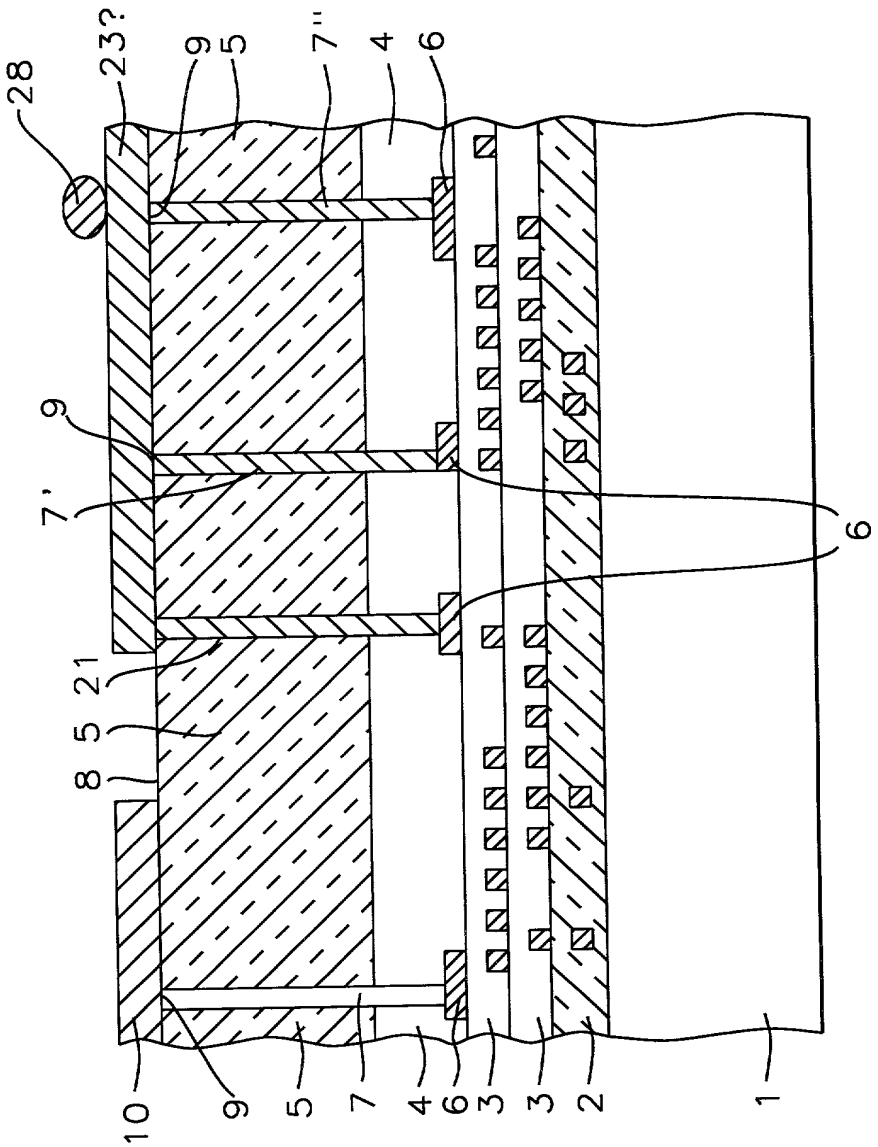

FIG. 7

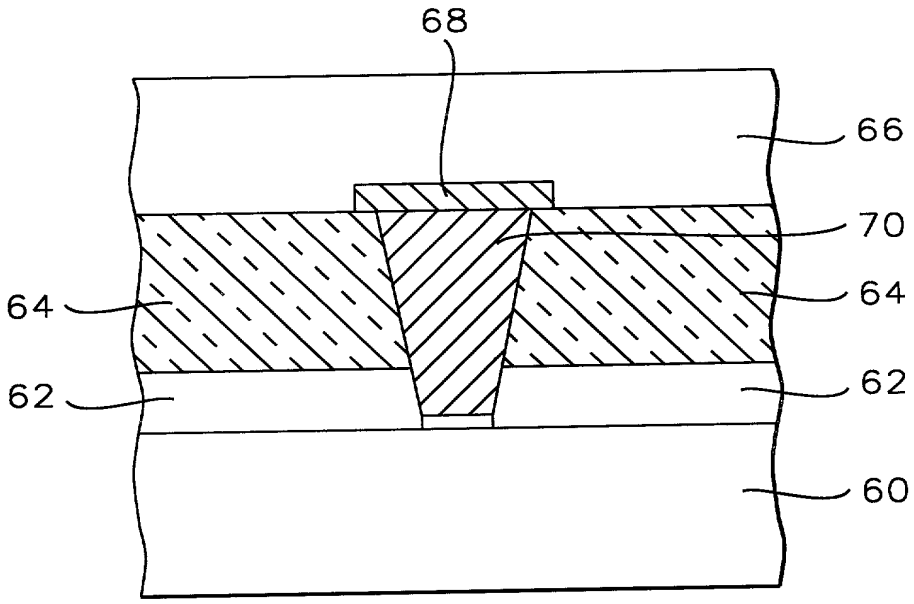
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FIG. 8

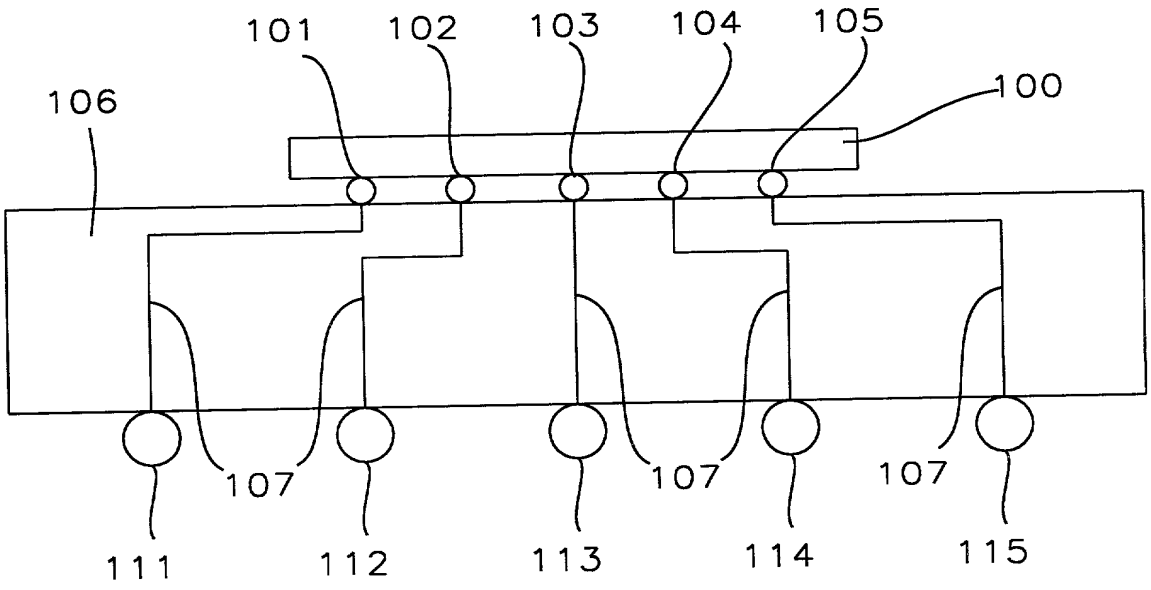
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FIG. 9

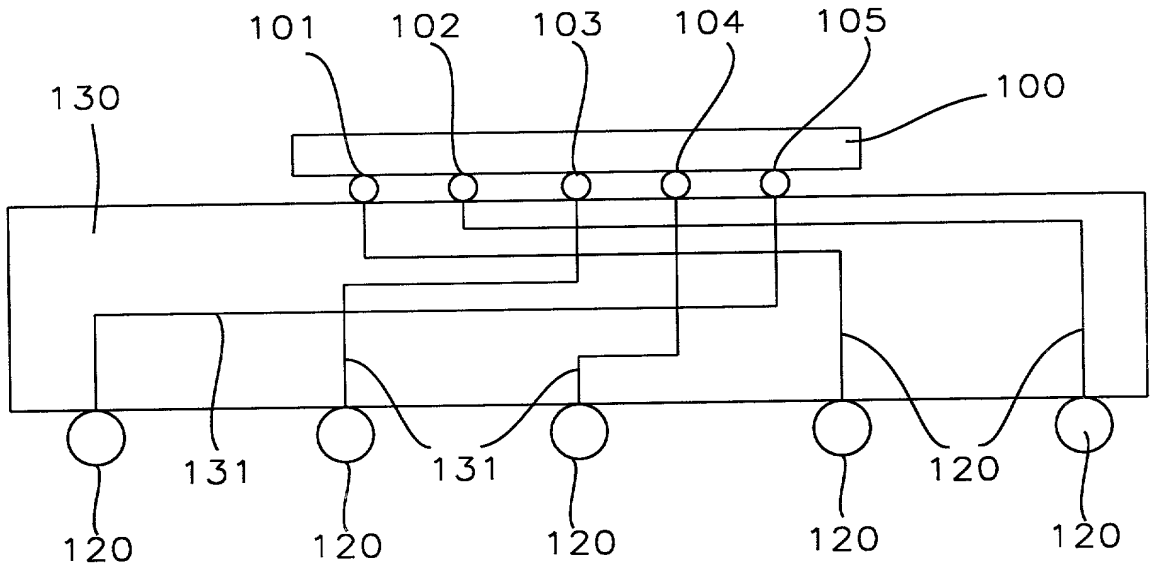
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FIG. 10

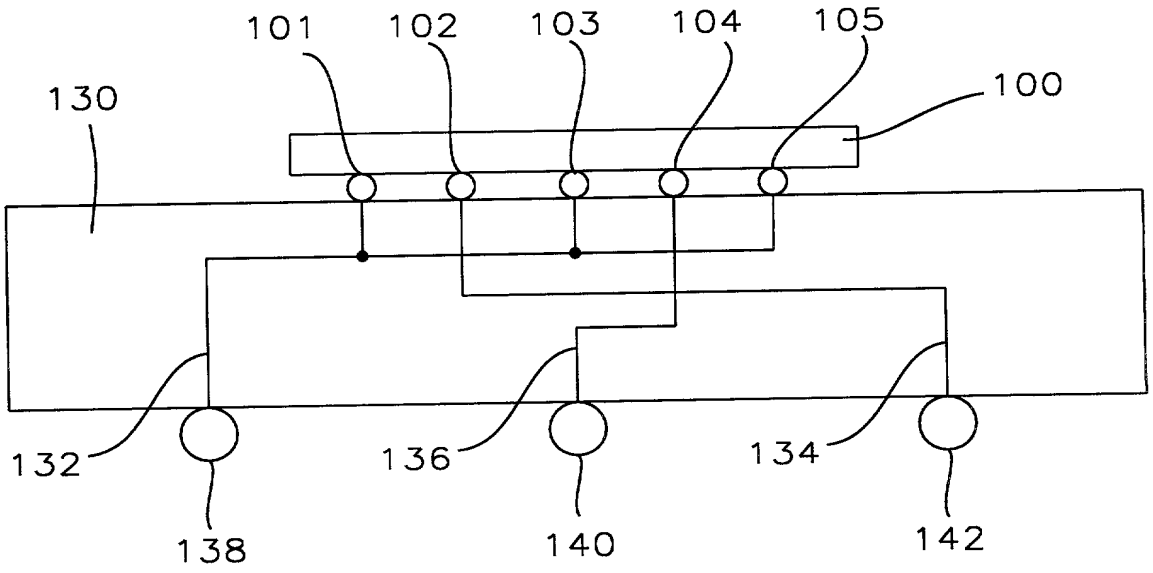
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FIG. 11

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

DOCKET NO. **MSLIN98-002C**

As a below named Inventor, I hereby declare that

My residence, post office address and citizenship are as stated below next to my name:

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled **Top Layers Of Metal For High Performance ICs**

the specification of which (check one)

X is attached hereto.

was filed on _____

Application Serial No _____

and was amended on _____ (if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification including the claims, as amended by any amendment referred to above

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed

Prior Foreign Application(s)

		Priority Claimed
(Number)	(Country)	(Day/Month/Year Filed)
(Number)	(Country)	(Day/Month/Year Filed)

I hereby claim the benefit under Title 35, United States Code §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application

09/210,791	12/21/98	PENDING
(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith (list name & registration no.)

GEORGE 0. SAILE. (Reg. No. 19,572), STEPHEN B. ACKERMAN (Reg. No. 37,761)

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Full name of **sole or first** inventor

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